Topics for System-on-Chip Design Comprehensive Exam

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Digital Design Techniques

- Synchronous design
  - Clocks go to clocks
  - Resets go to resets
  - Data controls the state of flop
  - Timing requirements of synchronous design
- Interfacing between clock domains
  - Synchronization flops
  - Resolving metastable states
  - Assessing clock domain/signal characteristics
- Receiving and utilizing resets
  - Recognize resets may violate setup/hold
- Finite State Machine Design
  - Mealy/Moore machines
  - State Diagrams
  - State Tables

Good HDL practices

- Synchronous vs asynchronous modeling
- Proper design techniques for synthesis
- Structural vs. RTL coding
- Avoiding latch inference

System-on-a-chip (SOC) design concepts

- ASIC vs. SOC and distinctions between the two
- SOC processor based architecture concepts
- SOC bus structure – enabling all interfacing blocks to have a common electrical connection and protocol.
  - An example bus definition is AMBA which includes AHB, ASB & APB
  - Devices connected to bus are either masters or slaves
    - Masters initiate transfers
    - Slaves respond to master's requests
  - DMA (Direct Memory Access) is a common scheme for moving blocks of data in an SOC
- The SOC flow "sits" on top of the ASIC flow. To fully understand the SOC flow one must have a working knowledge of the ASIC flow
- ASIC FLOW
  - Product need defined by marketing
  - Performance requirements defined by systems engineers

- Chip (ASIC/SOC) specification defined by chip designers
- Every major milestone is accompanied by a design review where the community is able to comment on the direction being taken
- Systems engineers often create behavioral models (algorithms & data paths) to create “baseline files” or “golden vectors” for verify the correctness of the HDL implementation
- Each chip design is partitioned into major functional blocks
    - Intellectual Property (IP) is a functional block that is designed elsewhere and included into the design with minimal or no modification.
    - Functional blocks that are designed include major partitions of the chip and typically go down one or two levels of instantiation (HDL levels)
- Functional blocks are verified by test benches
    - Typically designed by the functional block designers
    - Usually discarded after device integration
    - Synthesis (map to gates) typically performed at block level to confirm correctness of design and basic timing capabilities
- All functional blocks & IP blocks are integrated at full chip assembly
    - Verification at chip level performed with test benches created by a separate verification team through simulation (independent verification)
    - Complete chip synthesis yields a netlist that is a functional equivalent of the HDL design except it is composed of the library elements from the target library
    - Correctness of the netlist performed by Logical Equivalence Checking (LEC) – do they “logically” represent the same thing?
- Test insertion at the netlist level
    - Full scan for manufacturing tests
    - Memory BIST for manufacturing test
    - JTAG/Boundary Scan/1149.1 for manufacturing tests and test access for In Circuit Emulators (ICE)
- Clock tree insertion assures that the clock skew throughout the chip does not cause the device to fail hold requirements
- Floorplanning allows the silicon design to be accomplished with the knowledge of how the physical interfaces of the device will be connected on the PCB.
- Layout includes place & route which accomplishes the physical design of the device
- Final timing analysis utilizes information derived from the place & route process to confirm the device will perform as expected with respect to the physical delays within the device
- Silicon fabrication process is checked by using vectors created by an Automatic Test Pattern Generator (ATPG) tool and is executed on a tester after the device is packaged.

- SOC Flow
  - Similar to ASIC flow
  - One of the partitioning tasks is to define which operations will be performed in hardware and which will be performed in software
  - Typically the majority of blocks being integrated into an SOC are IP blocks with the exception of any particular interfaces that this device may be required to support (this is considered to be the design house's "secret sauce" – what makes them different
  - Simulation now includes hardware/software co-simulation where the model of the design not only simulates the functionality of each of the particular blocks but also allows the processor to fetch and execute instructions
  - Once simulation is complete many SOCs are emulated by mapping the design to FPGAs and run
  - Hardware/Software Design Flow plus tools