Topics for MS Comprehensive Exam
Fundamentals of Computer Architecture
Updated June 2014

Text: Computer Organization and Design, Patterson & Hennessey, 5th Ed., Elsevier Inc., 2014. ISBN: 978−0−12−407726−3		
Topic	***Text Section Reference***	***Example Exercises***
Performance	1.6 (p.28), 1.10 (p.49)	1.5, 1.6, 1.11, 1.12, 1.13
Mips Instruction Set Architecture	2.4−2.8 (pp.73−106), 2.10 (p.111)	2.7, 2.12, 2.18, 2.21, 2.23, 2.26, 2.46
Computer Arithmetic	3.1− 3.4 (pp.178−196)	3.7, 3.11, 3.15, 3.20, 3.21,
Floating Point	3.5 (pp.196−222)	3.22, 3.23, 3.26
The Datapath	4.3−4.4(pp.251−272)	4.4,4.7
Pipelining	4.5−4.9(pp.272−324)	4.8, 4.9, 4.14, 4.16
Parallelism	4.10 (p.332)	4.18
Caches	5.1−5.4 (pp.374−418)	5.3, 5.5, 5.7
Dependability	5.5 (p.418)	5.8
Virtual Memory	5.7(p.427)	5.11, 5.12

The above table is meant to suggest the possible topics that you may be questioned on in the MS Exam. It is not probable that all topics will be present but a candidate ought to prepare for all these topics by re−reading the sections indicated and looking at the example problems indicated. Some of the exam questions used in the past bear a strong resemblance to those of the current exam. If the candidate finds that these problems are too difficult to do, he or she may want to sit in or re−take the CECS 341 or CECS 440 course. Instructors of the course are able to provide some limited help with the material but in no way are they to be asked to cover the entire content of a semester's course for you. Remember that the goal of the exam is to determine if you have workable knowledge of the fundamentals of the discipline (the most basic ideas) and not of vague or esoteric topics.

Sample Questions from Previous MS Exam:

EX #1: A bench mark program was compiled for two different instruction sets on two different processors. Processor 1 runs at 3.2 GHz and Processor 2 at 2.5GHz. The following data was collected and is shown in the tables. From this data, answer the questions below.

Program 1 ($5x10^8$ instructions) on Processor 1 (3.2 Ghz)					
Category of Instruction	***A***	***B***	***C***	***D***	***E***
Clocks /Instruction	1	3	2	4	2
Frequency of Instruction	15%	35%	25%	10%	15%

Program 1 ($3.2x10^8$ instructions) on Processor 2 (2.5 Ghz)					
Category of Instruction	***A***	***B***	***C***	***D***	***E***
Clocks /Instruction	2	2	3	2	1
Frequency of Instruction	25%	20%	30%	15%	10%

Complete the following table based on the above data:

Item	***Processor #1***	***Processor #2***	***Ratio (#1 / #2)***
Performance			
MIPS Rating			

Ex #2: The following is a repeating pattern of ten branch outcomes where T= branch taken and N=branch not taken. Assume this pattern is repeated very many times in the program.

T,T,N,N,N,T,T,T,N,T

_____ (a) What is the accuracy of always-taken branch predictor for this series of outcomes?

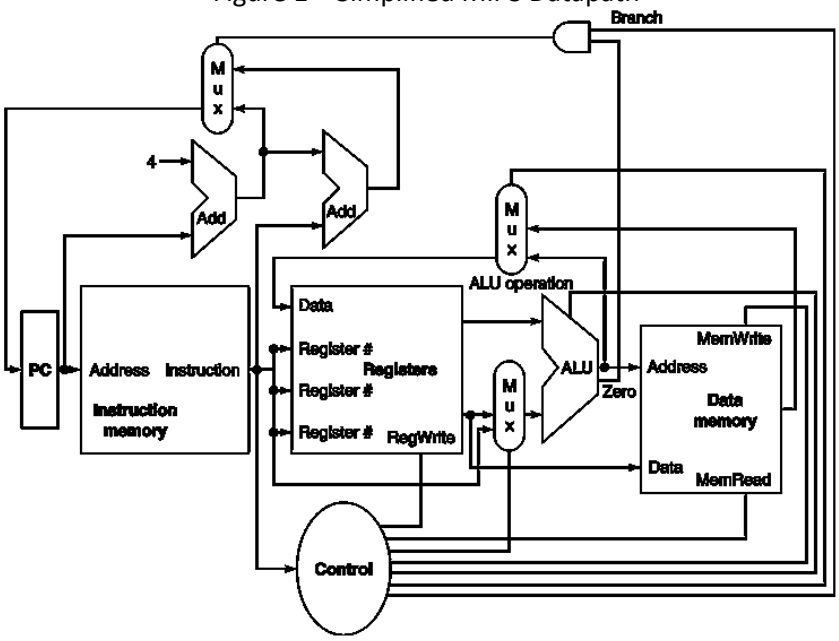
_____ (b) What is the accuracy of always-not-taken branch predictor for this series of outcomes?

_____ (c) What is the accuracy of the 1-bit branch predictor for this series of outcomes if the processor is initially in the taken state?

_____ (d) What is the accuracy of the 2-bit branch predictor for this series of outcomes if the processor is initially in the weakly taken state?

Ex #3: In the basic implementation of the MIPS datapath shown, there are seven kinds of major blocks. Different execution units and blocks of digital logic have different latencies. Latencies of blocks along critical path (longest latency) path for an instruction determine the minimum latency of that instruction. Control includes the latency for the main and ALU control units.

Figure 1 – Simplified MIPS Datapath



Assume the following resource latencies for two different hardware implementations given in picoseconds:

#	I-Mem	Add	Mux	ALU	Regs	D-Mem	Control
1	400	100	30	120	200	350	100
2	500	150	100	180	220	1000	65

_____ (a) What is the critical path (measured in ps) for a MIPS ADD instruction using (#2)?

_____ (b) What is the critical path (measured in ps) for a MIPS load instruction using (#1)?

_____ (c) What is the critical path (measured in ps) for a MIPS beq instruction using (#2)?

_____ (d) What would be the ratio of the maximum clock rate of data path #1 to #2?

Ex #4: Draw a picture of these following cache configurations and compute the hit rates for a series of memory byte accesses whose addresses are 6,8,0,3,6,1,2,9,0, and 10 for each cache configuration. In your diagrams show the final contents of the caches indicating the byte data found at memory location x as M[x].

(a) an 8 block direct mapped cache that uses 4-byte blocks
(b) a 8 block 2−way set associative cache that uses 1−byte blocks
(c) a fully associative 8 block cache that uses 2−byte blocks