Solutions

The AVR Microcontroller and Assembly Language Programming

1. With respect to the functional layout of data and program memory, which architecture, Charles Babbage's mechanical Analytical Engine designed in 1833 or Dr. John Von Neumann's electronic EDVAC computer designed over 100 years later in 1943, most closely resemble the AVR and why?

   The Analytical Engine designed in 1833 and the EDVAC designed in 1943 have the same five (5) principle organs that make up all modern day computers (Control, ALU, Memory, Input, and Output). Functionally, the main difference, other than the names given to each organ by Charles Babbage and Dr. Von Neumann, is the way data and instructions are stored. The Analytical Engine has a separate set of punched cards for data and the program. In contrast, both data and programs are stored together within the EDVAC's ultrasonic delay line memory. Like the Analytical Engine, the AVR architecture separates Flash program and SRAM data memory and therefore is more like the Analytical Engine. Today this is known as the Harvard Memory Model.

2. What is the address of the last byte in memory of a computer system with an 18-bit address bus and an 8-bit data bus?

   $2^{18} - 1 = 262{,}143_{10}$

   Range of addresses is 00000_{16} to $3FFFF_{16}$

3. What is the maximum number of characters that can be represented by an 8-bit code?

   $2^n = 2^8 = 256$ characters

4. What is the largest unsigned number, in decimal, that can be held in an 8-bit register?

   $2^8 - 1 = 255_{10}$

5. What is the range of signed 2's compliment numbers, in decimal, that can be held in an 8-bit register?

   $-2^{n-1} \not\subset 2^{n-1} - 1 = -128_{10}$ to 127_{10}

6. Convert 35_{10} to binary and hex.

   Using successive division:

   $35_{10} - 2 \times 16 = 3$

   $2 - 0 \times 16 = 2$

   0

   $23_{16} = 10\ 0011_2$

7. Convert 35_{16} to decimal.

   $3 \times 16^1 = 48$
   $5 \times 16^0 = 5$

   $48 + 5 = 53_{10}$

8. Perform the hex subtraction 36Bh – F6h.

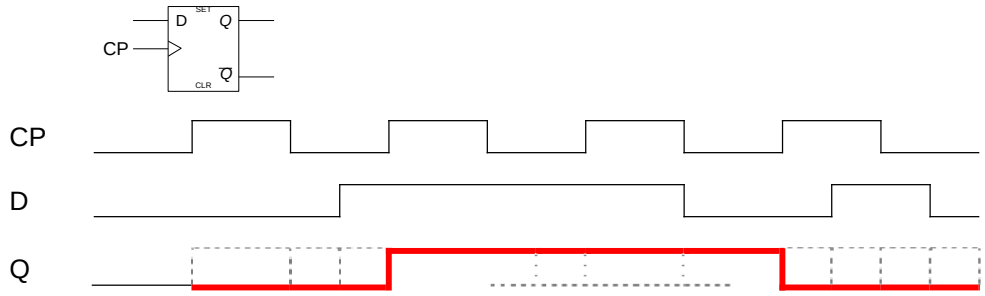
   $36B_{16}$
   $-\ F6_{16}$
   275_{16}

9. Applying DeMorgan's Theorem and the Basic Laws and Theorems of Boolean Algebra; simplify the following expressions:

$$\overline{\bar{a} + bc} = a(\bar{b} + \bar{c})$$

$$\overline{\bar{a} + \bar{b}} = a \cdot b$$

10. Complete the timing diagram for the following edge triggered D Flip-Flop. Q is initially at logic 0.



11. Assuming a 64-bit computer, for example the Intel Itanium microprocessor; place the following terms in ascending order relative to the number of binary digits they represent (Nibble, Word, Bit and Byte).

    Bit, Nibble (4 bits), Byte (8 bits), Word (64 bit architecture)

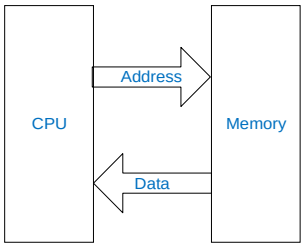
12. Which register in a CPU always contains an address? Program Counter (PC).

    What address is contained in this register? The program counter holds the address of the next instruction to be executed.

13. During an opcode fetch, what is the information on the address and data buses?

    The address bus contains the address of the next instruction to be executed (i.e. the contents of the program counter). The data bus then contains the actual instruction (i.e. the opcode) fetched from memory.

    What is the direction of information flow on these buses during an opcode fetch?



14. The sole purpose in life of a computer is to do what?

    The sole purpose in life of a computer is to *fetch* and *execute* instructions.

15. The Arduino Uno Board uses the Atmel Atmega328P microcontroller. Use the web to complete the following table.

Feature	ATtiny24	ATmega328P	ATmega644P
Flash Program Memory	2KBytes	32KBytes	64Kbytes
SRAM Data Memory	128 bytes	2 KBytes	4 KBytes

EEPROM	128	1 KBytes	2 KBytes
Timers (8 and 16 bit)	2	3	3
I/O pins	12	23	32
Serial peripherals (UART, USART, USI, SPI)	2	2	3
10-bit A/D channels	8	8	8

AVR Assembly Language Programming

16. List all AVR ISA (Instruction Set Architecture) registers.

    Program Counter (PC)

    General Purpose Registers R0 thru R31

    Status Register (SREG)

    Stack Pointer (SP)

17. For the three addressing modes listed, indicate where the data is located and at what address.

Addressing Mode	Data is located here	ATmega328P Address Space
Register	CPU	00_{16} – $1F_{16}$ (R0 – R31)
Immediate	Flash Program Memory	0000_{16} – $03FF_{16}$
Direct	SRAM Data Memory	0000_{16} to $08FF_{16}$
	I/O	0000_{16} to $003F_{16}$