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Debounce Circuit

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The circuit, shown in figure 1 (Breadboard on CSULB shield) , was designed to filter out the mechanical ringing (switching from close and open while the button is pressed) that a mechanical bush button will output while it is pushed.

The debounce design is centered on the 74LS74 D flip flop. The 74LS74 contains 2 D postive-edge - triggered-flip flops. Per the data sheet **(2)**, when the preset or clear inputs (active low) are low the outputs are set or reset disregarding the clock and D inputs. When the preset and clear inputs are both high, the output (Q, ~Q) the state of D input Is transferred when the clock pulse is on its positive edge. The outputs will not change to the D input's state until the next postive edge clock pulse (see function table below). Therefore, the D input can be changing states during that period without changing the output. A simulation on how the d flip flop works was performed using simulation software Multism (see graph 1). The circuit constructed on the breadboard was drawn. To clock the flip flop a function generator was used (4Hz clock, 5V pk voltage, 0 offset, 50% duty cycle). As shown on the graph the output (green waveform) follows the state of the input (the button is pressed (blue waveform)) on the postive edge of the clock (red waveform). Any bouncing that will take place during the 250mS interval will not affect the output.
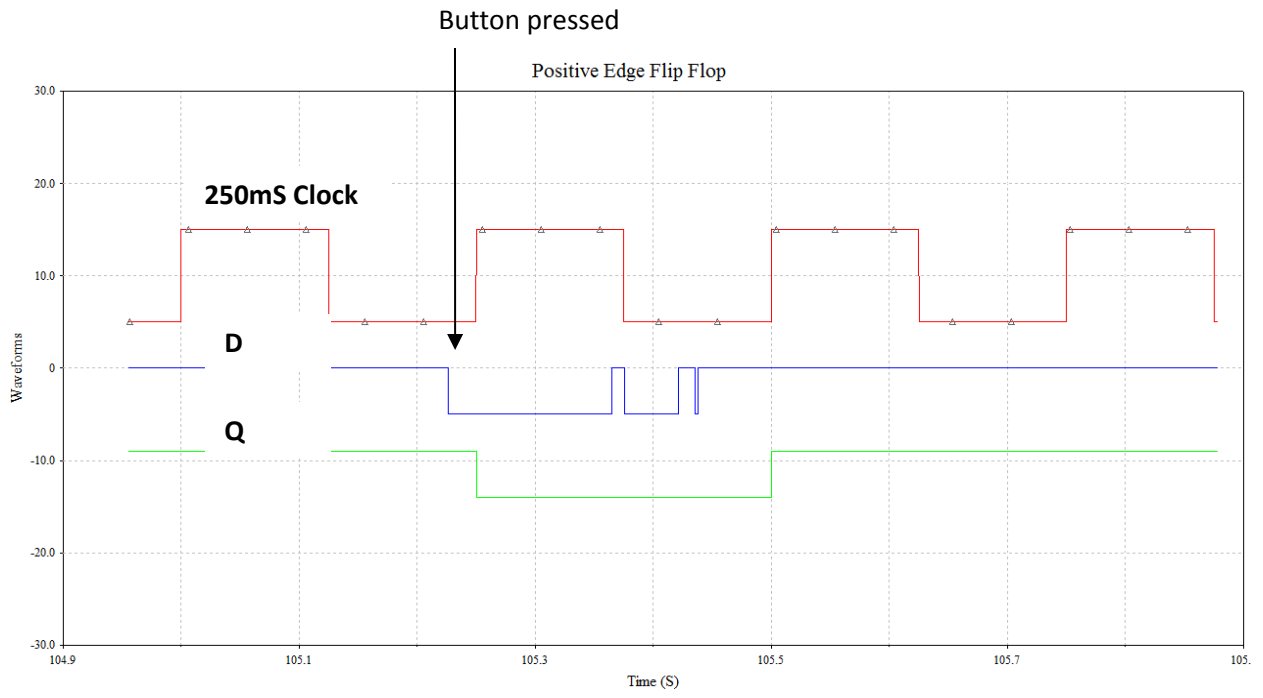
The key in the design is to filter out the bouncing states that the button generates so that the input port of the a digital circuit reads a stable logic state. Once the button is de-pressed the flip flop will register a logic 0 to its output , but will not see the the rest of pulses that are contributed by the mechanical opening and closing of the button contacts that usually last for about 20mS **(1)**. In this design the d flip flop is clocked with a pulse generated by the GPIO port of a microcontroller. The input clock has a period of about 250mS or frequency of 4Hz. This time is much larger than the 20mS so it can isolate any bouncing pulses that are needed to be filtered out from the input to the digital device.

The resistors on the debouncing circuit as shown are chosen to be a low value (2.2K ohm) to speed up the rise and fall times of the input. For the target microcontorller, the input ports could not have more than 20nS of rise and fall times since their input ports are characterized as capacitive in the vicinity of 10pF. With the 74LS74 having 2.2k ohm resistors, the time constant will be lower.

INPUTS				OUTPUTS	
~PRE	~CLR	CLK	D	Q	`Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Qo	~Qo

74LS74 Function Table

April 26, 2008

Button pressed

Graph 1

Read Latch

VCC
5V
VCC

5

U5B
74126N   U2A

Internal
CPU BUS   ~1PR
4   1D   1Q   5

15   1CLK   ~1Q   6   6   Q1
                                                    IRF250
Write to   0
Latch   ~1CLR
                                          7474N

Read Pin

3

U4A
74126N   8051

~INT0   P3.2 pin

F
1   Rl

Read Latch

VCC
5V
VCC

U6A
74126N   U3A

Internal   9
CPU BUS   ~1PR
10   1D   1Q   5

12   1CLK   ~1Q   6   8   Q2
                                                    IRF250
Write to   ~1CLR   0
Latch   7474N

Read Pin

7

U7A
74126N

F
1   Rl

1ff_clk

P3.7 pin

VCC   VCC
5V   5V
VCC   VCC

R1   R2
2.2kΩ   2.2kΩ

2   U1A

~1CLR

~1Q   1CLK   3

1Q   1D   2   1   J1

~1PR   Key = A   0

7474N

13   11
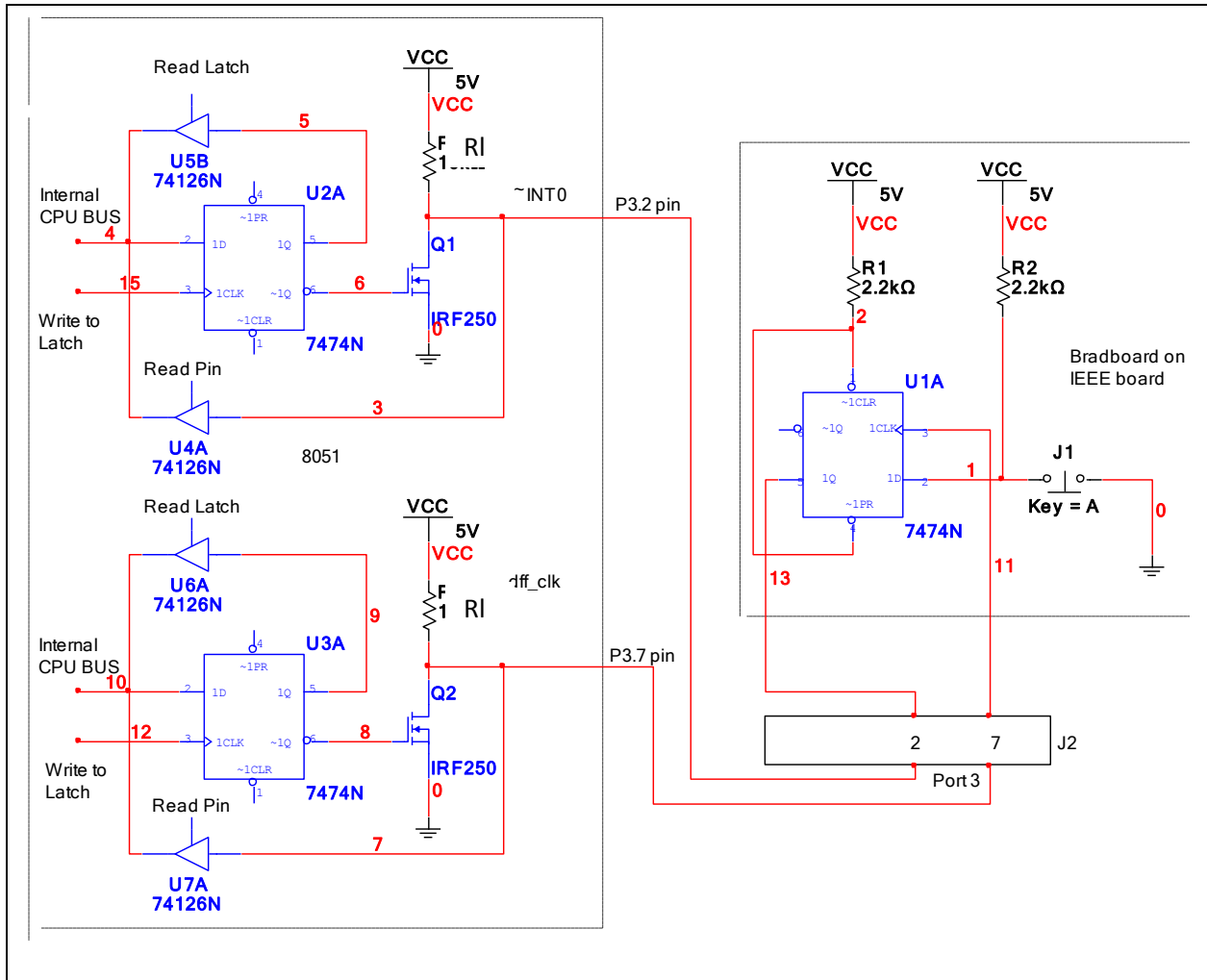
Bradboard on
IEEE board

2   7   J2

Port 3

Figure 1

(1) http://www.patchn.com/index.php?option=com_content&task=view&id=59&Itemid=36
(2) http://www.fairchildsemi.com/ds/DM/DM74ALS74A.pdf