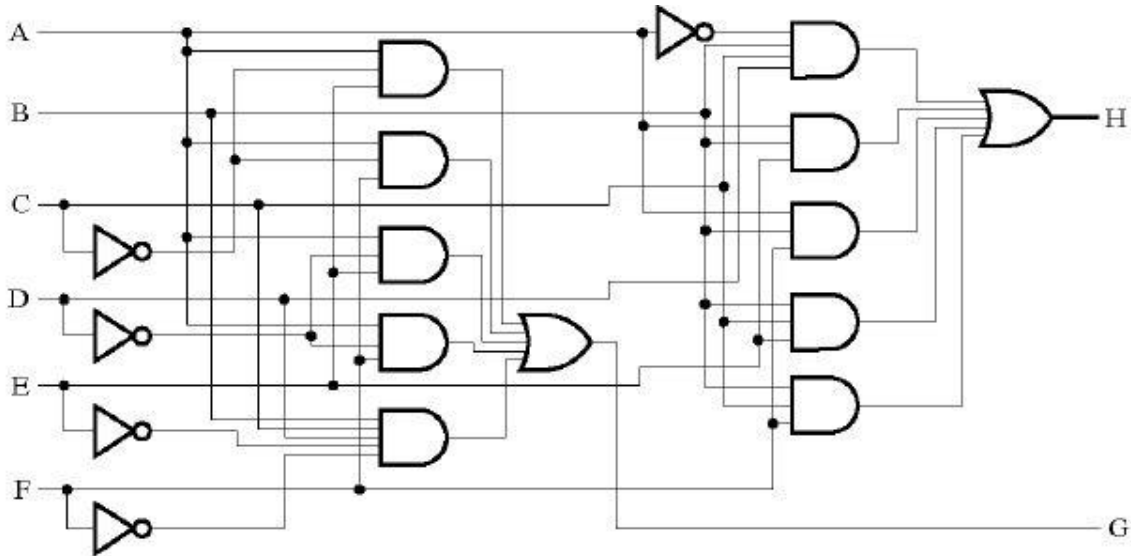
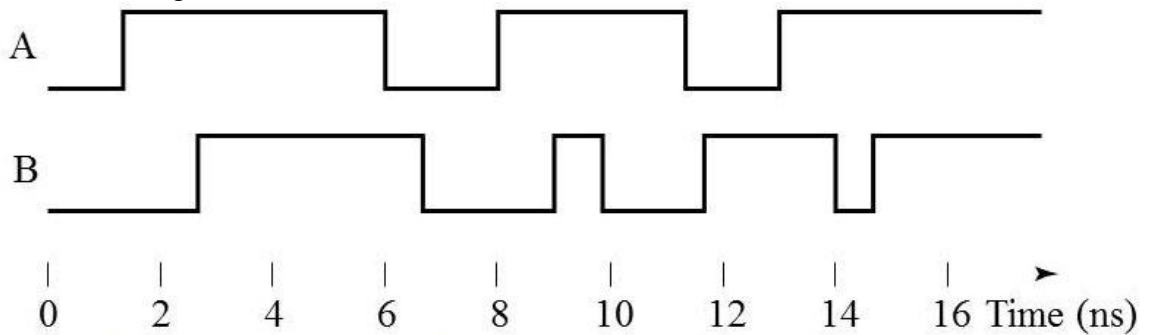


- 1 Simplify the following Boolean functions by means of a three-variable map:
(a) $F(X, Y, Z) = \sum m(1, 3, 6, 7)$ (b) $F(A, B, C) = \sum m(0, 1, 2, 4, 6)$
- 2 Simplify the following Boolean Expressions using a map
(a) $\bar{X} \cdot \bar{Z} + Y \cdot \bar{Z} + X \cdot Y \cdot Z$ (b) $\bar{A} \cdot B + \bar{B} \cdot C + \bar{A} \cdot \bar{B} \cdot \bar{C}$
- 3 Simplify the following Boolean expressions, using a map
(a) $F(W, X, Y, Z) = \sum m(0, 2, 5, 8, 9, 11, 12, 13)$
(b) $F(W, X, Y, Z) = \sum m(3, 4, 6, 7, 9, 12, 13, 14, 15)$
- 4 Find the minterms of the following expressions by first plotting each expression on a map:
(a) $F(W, X, Y, Z) = X \cdot Y + X \cdot Z + \bar{X} \cdot Y \cdot Z$
(b) $F(A, B, C, D) = \bar{B} \cdot \bar{D} + A \cdot B \cdot D + \bar{A} \cdot B \cdot C$
- 5 Simplify the following Boolean functions by finding all prime implicants and essential prime implicants and applying the selection rule:
(a) $F(W, X, Y, Z) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$
(b) $F(A, B, C, D) = \sum m(1, 3, 4, 5, 7, 8, 9, 12)$
- 6 Simplify the following Boolean functions in product-of-sums form:
(a) $F(W, X, Y, Z) = \sum m(0, 1, 2, 6, 8, 9, 10, 13)$
(b) $F(A, B, C, D) = \prod M(1, 3, 5, 6, 7, 9, 10, 11, 14)$
- 7 Simplify the following Boolean functions F together with the don't-care conditions d . Find all prime and essential prime implicants and apply the selection rule.
 $F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15)$, $d(A, B, C, D) = \sum m(2, 3, 5, 10, 11, 14)$
- 8 An integrated circuit logic family has NAND gates with a fan-out of 8 standard loads and buffers with a fan-out of 16 standard loads. Show how the output signal of a single NAND gate can be applied to 38 other gate inputs using buffers. Assume that each input is one standard load.

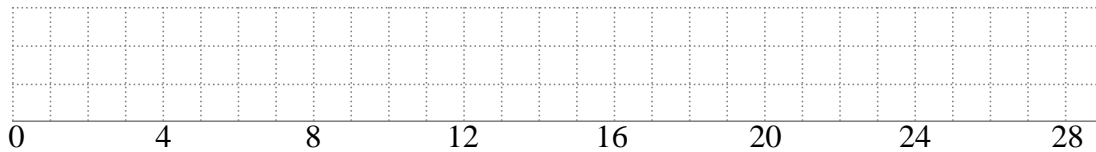
- 9 The gates including inverters in the figure below have propagation delays of $t_{pd} = 0.5 \text{ ns}$. What is the propagation delay of the longest path through the circuit?



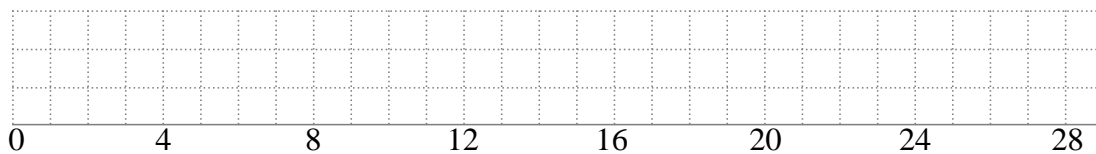
- 10 The waveform in the figure below is applied to an AND gate. Find the output of the AND gate assuming that:



- (a) it has no delay.



- (b) it has a transport delay of 2 ns.



(c) it has an inertial delay of 2 ns with a rejection time of 1 ns.

