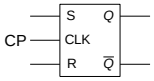
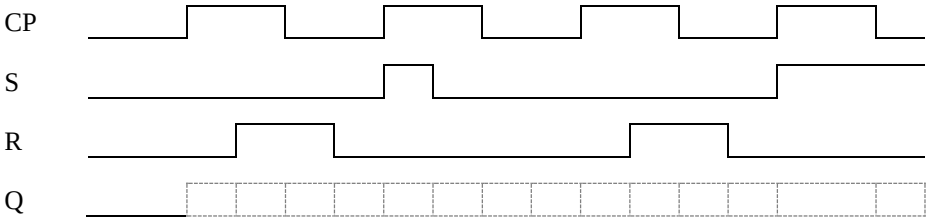
EE201 Flip-Flop Worksheet

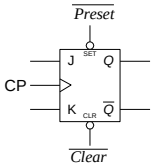
1. Complete the characteristic table and timing diagram for the following level triggered RS Latch. Q is initially at logic 0. Under "Action," for each row insert one of the following:
a) don't change, b) toggle, c) set , d) reset, e) undefined



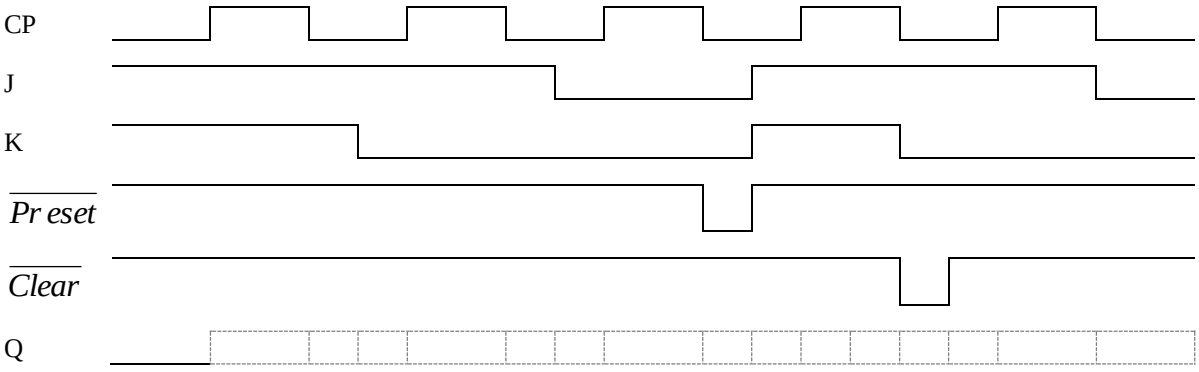
RS Flip-Flop			
S	R	Q_{t+1}	Action
0	0	Q_t	a) don't change
0	1		
1	0		
1	1		



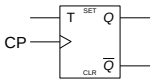
2. Complete the characteristic table and timing diagram for the following edge triggered JK Flip-Flop. Under "Action," for each row insert one of the following: a) don't change, b) toggle, c) set , d) reset, e) undefined. Both preset and clear signals are asynchronous with respect to the clock.



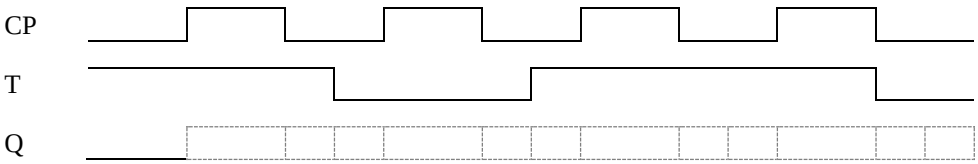
JK Flip-Flop			
J	K	Q_{t+1}	Action
0	0		
0	1		
1	0		
1	1		



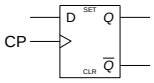
3. Complete the characteristic table and timing diagram for the following edge triggered T Flip-Flop. Q is initially at logic 0. Under "Action," for each row insert one of the following:
a) don't change, b) toggle, c) set , d) reset, e) undefined



T Flip-Flop		
T	Q_{t+1}	Action
0		
1		



4. Complete the characteristic table and timing diagram for the following edge triggered D Flip-Flop. Q is initially at logic 0. Under "Action," for each row insert one of the following:
a) don't change, b) toggle, c) set , d) reset, e) undefined



D Flip-Flop		
D	Q_{t+1}	Action
0		
1