EE 201-03
(19468)

Digital Logic Design

Practical design of digital circuits. Basic topics in combinational and sequential logic with applications to the design of digital devices.

Syllabus

This course is for everyone who wants to design and build digital circuits. The material presented is at the introductory course level for electrical engineering (EE) students. The course will provide you with a solid foundation in combinational switching circuits as well as the basic concepts involved in sequential circuit design. Once obtained, these principals lay the groundwork for understanding the organization and design of digital systems.

The labs are designed to help you grasp the fundamentals and understand how things work in the real world. You will be working with SSI ICs and Field Programmable Gate Array (FPGA) hardware implementations using Computer Aided Design (CAD) and Electronic Design Automation (EDA) software tools.

Subjects Covered in Class

Introductions — What is Digital Logic Design? The Difference between an Analog and a Digital System

Number Systems — Positional Notation (Decimal, Binary, Octal, and Hexadecimal), Nomenclature, Converting Between Number Systems, Binary Arithmetic (Subtraction with Complements), Binary Codes (BCD, Error-Detection, Gray, and ASCII)

Boolean Algebra — Binary Operations (AND, OR, NOT), Basic Laws, Proof by Perfect Induction, De Morgan's Theorem, Canonical and Standard Forms (SOP, POS).

Simplification of Boolean Functions — Karnaugh Maps of up to four (4) variables, Product-of-Sums, and Don't Care Conditions

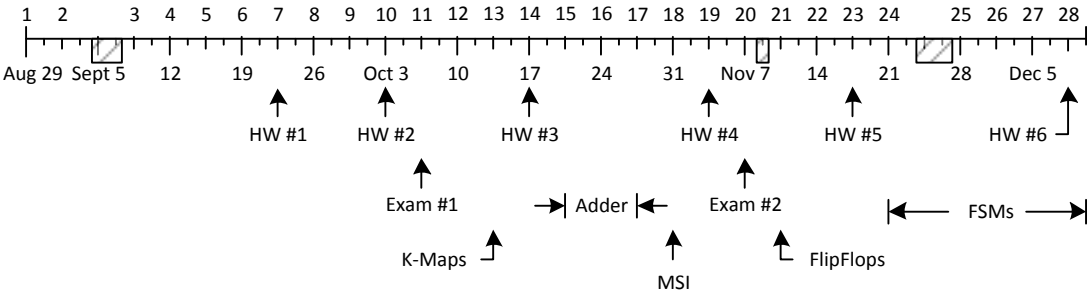
Design Hierarchy — Analysis and Design Procedure, Electronic Design Automation (EDA) and Hardware Description Languages (HDLs), Design Example: A Binary Adder, Digital Building Blocks (Decoders, Encoders, Multiplexers, and Demultiplexers)

Registers and Counters — Shift Registers with Parallel Load, Asynchronous (Ripple) and Synchronous Binary Counters

An Introduction to State Machine Design — Combinational versus Sequential Design, Switch Debounce Circuit (RS Latch), Flip-Flops, What is a State Machine, State Machine Theory (State Diagram), Mealy, Moore, and One Hot State Models

Special Topics — How to implement Boolean functions based on a target VLSI device. ASIC and IC transistor type (TTL, CMOS). Implementing Boolean functions with decoders (RAM, ROM), and multiplexers (FPGA), PALs, and CPLDs.

Schedule



Homework

Homework problems will be provided by the instructor. Due dates will be approximately as shown in the timeline above. Actual due dates will be provided below as the course progresses.

Subject	Reading	Homework Number	Due Date
Introductions	Chapter 1	1	September 21st
Number Systems	Chapter 2		
Boolean Algebra	Chapter 3	2	October 3rd
Simplification of Boolean Functions	Chapter 4	3	October 17th
Digital Arithmetic and Design Hierarchy	Chapter 6	4	November 2nd
Flip-Flops and Related Devices	Chapter 5	5	November 16th
Counters and Registers plus Finite State Machine Design	Chapter 7-1 to 7-13	6	December 7th
	Chapter 7-14		
Design to Technology	Chapter 13		

Exams

I will try and provide exam questions which are based on material covered multiple times in the reading material, class, and lab; however, you are responsible for any material covered in class or lab. Please ask in class if you have any questions.

Exam	Date[1]	
Midterm # 1	Wednesday	October 5th
Midterm #2	Monday	November 7th
Final.	Wednesday	December 14th — 12:30 p.m. to 2:30 p.m.

[1] Dates, except final, are estimates only

Grading Procedure[2]

Category	Number	Weight %	Total %
Homework, Quizzes, Misc.	*Varies*	*Varies*	15
Midterms	2	15 / 20	25
Lab Projects	9	*Varies*	30
Final	1	30	30

Labs

TBD

Frequently Asked Questions:

Q. When and Where are homework and lab assignments due?

A. Place your homework and labs on my desk when you come into class. Homework and lab assignments are due at the BEGINNING of the class period on the due date. Turn in what you have when it is due.

Q. What if I am only 1 minute late to class, can I still turn in my assignment?

A. Late homework will not be accepted. Late lab assignments will be prorated by 10% per class for a period of two weeks after which the maximum grade you can receive is 5 points out of 20. Minutes, hours, and days do not count.

Q. What constitutes acceptable quality for lab assignments?

A. For lab assignments it means your lab report:

- covers material in the lab handout
- covers supplemental material discussed in the lab
- is properly formatted (see "*Instructions on the Preparation of Lab Reports*")
- demonstrates acceptable writing skills

Q. What constitutes acceptable quality for homework assignments?

A. For homework, it means putting forth a credible effort to solve each problem and providing the assignment in a clean, organized, and legible format (see "*Instructions on the Preparation of Homework Assignments*")

Q. An emergency came up that prevented me from taking an exam. Can I take a make-up exam?

A. Makeup exams (but not quizzes) may be taken if you received my permission PRIOR to the exam. Makeup exams will not be the same ones taken by the class; however, grading will be on the same curve.

[2] See University, College and Department rules for information on withdrawing from the class. I do not give incomplete (I) grades.

Contact Information

Instructor — G. C. Hill

Office — VEC 503-A

Hour(s) — Wednesday from 10:00 a.m. to 12:00 p.m.[3]

E-mail — hill@csulb.edu

Prerequisites

Math 117 — Precalculus

Class Meetings

Monday and Wednesday from 1:00 to 2:50 a.m. in ECS 316

Materials

Text Book — Digital Systems Principles and Applications, by Ronald J. Tocci, Neal S. Widmer, and Gregory L. Moss – 10th or 11th Edition.

Recommended Text Book – Logic and Computer Design Fundamentals – **3rd Edition**, by M. Morris Mano and Charles R. Kime

Lab Supplies

1. Lab Notebook (Composition Book with Grid Lines),
2. Computer Account (optional if you have a laptop)
3. Breadboard Kit
4. Digilent Nexys-2 FPGA Board

Instructions on the Preparation of Homework Assignments

Your **homework assignment** should be **stapled**. Do not use, folded corners, paper clips, three ring binders, and report covers. Place a **title block** with the following information in the upper-right hand corner of the first page: your name, the homework number, section number (and/or the days of the week and time the class meets), and date prepared. Include the number of and a **short synopsis of each question**. **Circle your answer**. Your homework solutions should progress from the top to the bottom of the page. Do not break the page into horizontal and vertical areas, where I need to search to find the solution. Your homework assignment may be written or typed. All material should be clean, organized, and **legible**!

Use **8½"x 11" white sheets of paper**. Do not use re-used paper or pages with ratty edges in your assignment. Each page should include a **page number**. Do not include superfluous and **redundant material**. This includes blank pieces of paper.

Instructions on the Preparation of Lab Reports

Your **lab report** should be **stapled**. Do not use, folded corners, paper clips, three ring binders, and report covers. The report should begin with the **title page/table of contents** provided with the lab

[3] If I am not in my office try the ECS 316 lab.

assignment. Complete the title page by typing your name, partner's name (if applicable), section number (and/or the days of the week and time the class meets), and date prepared. The table of contents lists each lab section followed by the page number where it begins. Do not change the page numbers on the right; your lab should fit within these constraints.

Written material should be **typed** and include descriptive headings. All **printouts** should be readable, have descriptive titles, and include comments (annotated) to help the reader interpret the information. Match the orientation (portrait and landscape) of your printouts to the format of the material. For example, schematics, waveforms, and listings (.LST files) should be output in landscape while source files (.ASM) should be output in portrait. Place landscape printouts in the report cover such that the top of the printout is closest to the staple.

Schematics should include a title block containing the name of the schematic, your name, and date. All **timing diagrams** should include a title (top and centered) containing the name of the corresponding schematic and the nature of the simulation run. Waveforms making up the timing diagram should be organized with the inputs on the top and the outputs on the bottom. Critical events shown by the waveforms should be annotated. For example an input event causing an unexpected output should be identified with corresponding timing information included.

All material should use 8½"x 11" white sheets of paper. Do not use re-used paper in your report. Each page should include a **page number**. Once again the page number should correspond to the one provided in the table of contents. Do not include superfluous and **redundant material**. This includes blank pieces of paper, schematics with no circuits, timing diagrams with no waveforms, etc. An example of redundant material would be two timing diagrams one without derived waveforms (busses) and the other with this information. Another example, would be a schematic with and without back annotation information. In this example, include only the schematic with back-annotated information. If you are in doubt ask the instructor.

Append in a clearly marked section (i.e., include a title page) a COPY of raw data used during the lab. This would include applicable pages of your **lab notebook**, notes, or original pseudo-code. Copies should be readable. Highlight all required signatures.